ABSTRACT

A processor is disclosed that executes an instruction including a user-defined value (an address or a command) and provides the user-defined value during execution of the instruction. In one embodiment the processor includes a bus interface adapted for coupling to a bus, and the processor drives the user-defined address or command upon one or more signal lines of the bus via the bus interface during execution of the instruction. A described data processing system includes the processor coupled to a device including an addressable register. The device receives a user-defined address from the processor and accesses the addressable register in response to the user-defined address. Methods are disclosed for obtaining a value stored in an addressable register, providing a value stored in an addressable register, storing a value in an addressable register, and modifying a value stored in an addressable register.